

 **WEST Search History** 

DATE: Thursday, September 19, 2002

**Set Name** **Query**  
side by side**Hit Count** **Set Name**  
result set*DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=OR*

L3 BGA and (bumps with tolera\$4 with stress\$3)

0 L3

*DB=USPT; PLUR=YES; OP=OR*

L2 BGA and (arrang\$5 with stress)

65 L2

L1 BGA with (stress adj tolerant)

0 L1

END OF SEARCH HISTORY

**WEST**

Generate Collection

L2: Entry 52 of 65

File: USPT

Dec 28, 1999

DOCUMENT-IDENTIFIER: US 6008543 A

TITLE: Conductive bumps on pads for flip chip application

Brief Summary Text (4):

A method of mounting semiconductor elements on a circuit board has been known, wherein semiconductor elements are covered with a ceramic or plastic package for protection from an external environment, and are mounted on the circuit board using terminals protruded therefrom. In recent years, a BGA package has been emerged to further increase the high mounting density, and further, an examination has been actively made to put to practical use a flip chip mounting technique for forming bumps on a chip (semiconductor element) and connecting the chip on a circuit board through bumps in a face-down manner.

Brief Summary Text (15):

A method of relaxing a thermal stress due to differences in linear expansion coefficients has been known, wherein bumps are arranged in a staggered manner for dispersing stress concentration applied to bumps [Soga et al.: Journal of Japanese Institute of Electronic Information Communication vol. J70-C, No. 12 (December, 1987), pp. 1575-1582]. In this case, however, for a given number of output terminals, an layout area of the semiconductor element having Al pads that are arranged in a staggered manner must be made larger than that of a semiconductor element having Al pads arranged in rows and columns at nearly equal intervals. This is undesirable in terms of cost and mounting density.

09/832, 884